On the Development of a High Efficiency 750 GHz Frequency Tripler for THz Heterodyne Systems

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Abstract—**The development of a 750 GHz Schottky varactor diode frequency tripler having a measured output power and efficiency of more than 120 μW and 0.8% at a frequency of 803 GHz is described. The output powers and efficiencies are the highest reported for this frequency. The 750 GHz tripler mount is analyzed and optimized using a scaled model of the mount. Measurements of the embedding impedance seen by the device, using the model, are compared with theoretical values.**

Introduction

Due to the interest of developing superconducting mixers, such as SIS-mixers, at frequencies around 1 THz [1], the demand for solid state local oscillators has been steadily increasing. In 1988 Farran Technology was commissioned by the European Space Agency to investigate and develop solid state sources based on Schottky diode multipliers to be used as local oscillators in such receivers. One of the targets has been to develop a 750 GHz solid state source with a predicted output power of ≥50 μW based on two triplers pumped by an 83 GHz InP-TED oscillator. This paper reports on the progress and results in developing the tripler between 250 GHz and 750 GHz. The mechanical design of the tripler has been based on the concept by Erickson [2], for submillimeter-wave multipliers.

Theoretical Study and Mount Design

Using a large signal multiplier analysis program based on the principle of harmonic balance developed by Siegel *et al.* [3], different Schottky varactor diodes having a zero voltage junction capacitance $C_j(0) = 1.6$ to 3.4 fF were investigated for the tripler, see Fig. 1. The input power was varied between 1–6 mW since this was estimated to be the available output power from a 250 GHz tripler [4] used as the pump source for the 750 GHz tripler. The description of the devices used in the simulation was simplified in that a fixed epitaxial layer thickness and doping

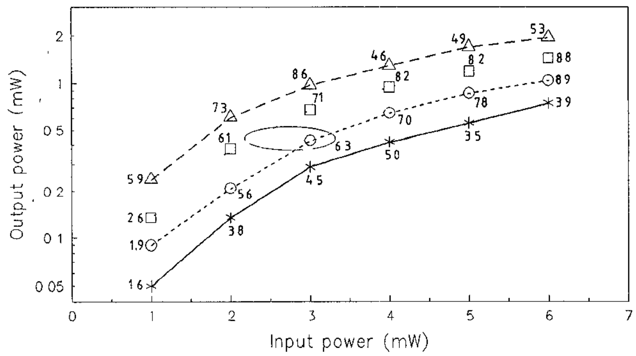

Fig. 1. Calculated output power as a function of input power for Schottky varactor diodes having a capacitance $C_j(0)$ of between 1.6–3.4 fF. The bias voltage is optimized for best efficiency. The numbers along the curves are the maximum voltages V_{max} across the device at the particular operating point. (△): $C_j(0)$ is 1.6 fF, $V_b = 4$ V. (□): $C_j(0)$ is 2.2 fF, $V_b = 6$ V. (*o*): $C_j(0)$ is 2.8 fF, $V_b = 6.5$ V. (*x*): $C_j(0)$ is 3.4 fF, $V_b = 7$ V.

of 0.49 μm and 9 10^{16} cm^{-3} respectively was used for the low doped epitaxial region, for all the devices. Later investigation on realizable Schottky diodes has shown that a epitaxial layer thickness and doping of between 0.35–0.25 μm and 1.5–3.5 10^{17} cm^{-3} is probably more appropriate for devices having a $C_j(0)$ of 3.4 to 1.6 fF. The values for the epitaxial layer thickness and the doping have a minor influence on the series resistance of the devices only when the epitaxial region is not fully depleted. Thus in the calculations the length and doping of the epitaxial layer was fixed for the devices, and the epitaxial layer was assumed to be fully depleted. In the calculation, also the series resistance R_s of the device was set to a fixed value of 20 Ω, which falls between calculated values for R_s of 18.8–24.3 Ω for realizable diodes having a $C_j(0)$ of 3.4 to 1.6 fF.

The marked region in Fig. 1 shows the operating condition when the maximum voltage V_{max}, that is the bias voltage plus the peak rf-voltage, is approximately equal to the breakdown voltage V_b. The breakdown voltage V_b is the calculated breakdown voltage for realizable Schottky diodes, see above, having the same junction capacitance $C_j(0)$ and close to the same series resistance R_s as for the ones used in the simulation. The breakdown voltage V_b for realizable Schottky diodes was found to vary between 4–7 V, for diodes having a $C_j(0)$ of 1.6–3.4 fF. The big change in maximum voltage V_{max} across the devices having a $C_j(0)$ of 1.6 and 3.4 fF for input powers of 4 and 5 mW respectively is due to a change in bias

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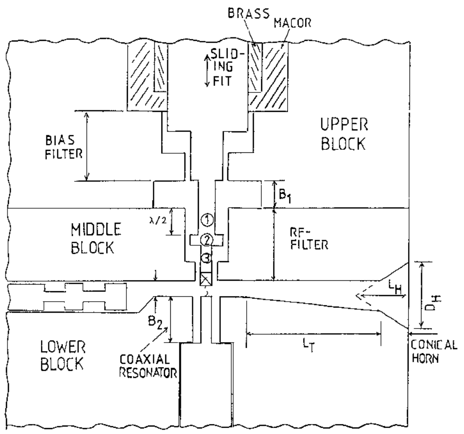

Fig. 2. Cross-sectional view of the 750 GHz tripler. (Not to scale). B_1 = 0.091 mm, B_2 = 0.041 mm, $L_H = 2\lambda$, $D_H = 2.54\lambda$, $L_T = 5\lambda$.

voltage, in order to find the optimum operating point for the particular input power. The bias voltage used in the simulation varied between 0–2 V. From Fig. 1 it can be seen that diodes with a capacitance between 2.2 to 2.8 fF should be the most suitable ones. The device capacitance was chosen to be 2.8 fF. The calculated output power for such a device is about 500 μW, see Fig. 1. This allows for 10 dB matching and circuit losses, yielding the required output power of ≥ 50 μW. Experimental results have shown that twice the pump power needed for $V_{\max}$ to reach V_b can be used [4]. Therefore it should be possible to use a pump power of approximately 5 mW thereby increasing the output power before power saturation of the device occurs.

A cross section view of the 750 GHz tripler is shown in Fig. 2. The function of the coaxial resonator used in the multiplier, see Fig. 2, is based on the principle developed by Ericsson [4]. The step in the outer diameter of the coaxial resonator is incorporated in order to achieve a better short circuit at the end of the idler [2]. The input waveguide is a reduced height WR-3 waveguide. The wide dimension of the output waveguide is 0.258 mm, thus being cutoff at 581 GHz. Due to the very small height of the output waveguide at the position of the device, being only 0.041 mm, see Fig. 2, a normal backshort consisting of high and low impedance sections could not be incorporated close to the device. To allow for such a backshort the reduced waveguide height was tapered up to full height behind the device, see Fig. 2. Scaled model measurements showed that the output backshort functioned well over the important operating frequency range. A conical horn was used for the output port due to the ease with which it could be machined. By proper selection of the length of the horn and the horn opening it is possible to have a nearly identical beam pattern in the E and H planes [6]. The waveguide is matched to the horn using a 5λ long taper with a square cross-section at the horn throat, having the same cutoff frequency as the circular horn throat. Thus the impedance discontinuity between the horn and the waveguide becomes small [2].

A scaled model of the mount (scaling factor = 83.31) was designed in order to investigate and optimize the embedding impedances seen at the input, idler and output frequencies by the diode.

Using the scaled model it was found that most resonances in the embedding impedance were due to higher order mode excitation in the rf-filter, see Fig. 2. These resonances were particularly strong close to the cutoff frequency for the particular mode. Due to mechanical limitations it was not possible to shift the coaxial TE_{11}-mode cutoff frequencies for the rf-filter above the highest operating frequency except for the last rf-filter section. The TE_{11}-mode and TE_{21}-mode cutoff frequencies for the other filter sections, that is Sections 1, 2, and 3 in Fig. 2, were instead shifted to the frequency region between the input and the idler frequency, and idler and output frequency respectively, thereby minimizing the influence of the resonances related to the cutoff frequencies for the modes. The rf-filter is extended by a $\lambda/2$ coaxial section, part of Section I in Fig. 2, in order to make the middle block easier to machine, see Fig. 2 [2].

A theoretical model was developed for the mount, where the coupling between the rf-filter and the input waveguide was calculated using the theory by Williamson [7]. For the output port a simplified theoretical model was used based on the assumption that the embedding impedance seen by the diode is the sum of the impedances from (i) the output waveguide in parallel with the backshort, (ii) the rf-filter and (iii) the idler [8]. Though this simplified model is not sufficient in fully describing the output port it was used in the absence of a more accurate one. The bias filter was assumed to present a short circuit at the input frequency.

Using the theoretical and the scaled models of the mount the embedding impedances seen by the device at the input, idler and output frequencies were calculated and measured respectively, see Fig. 3. The bias filter was short circuited in the measurements.

It can be seen in Fig. 3 that there is a difference mainly in reactance between the measurements and the calculated values. The discrepancy in reactance is believed to be partly related to the simplifications in the theoretical model used in the calculations. The increased capacitance due to the measurement cable-waveguide junction compared to the actual mount was found to add a capacitance of only about 43 fF to the actual values. Thus this capacitance does not account for the noted discrepancy.

In Fig. 3 is also plotted the complex conjugate of the diode impedance, Z_d^*, or the reactance X_d^*, at the input, idler and output frequencies for the 2.8 fF diode. Comparison between Z_d^* or X_d^* and the measured impedances shows that a match to the device could be achieved at the high frequency end of the output frequency range 675–825 GHz wanted for the tripler.

Simulations using the theoretical model of the mount gave a maximum efficiency for the tripler of 11% at 750 GHz, compared to the theoretical value of 12.2% found in the diode simulations for 2.5 mW input power.

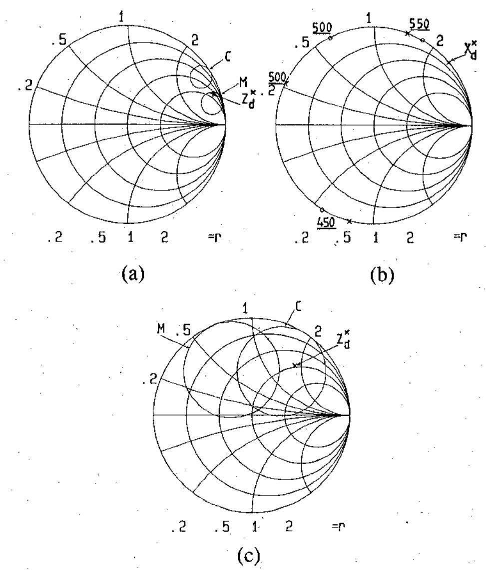

Fig. 3. Measured and calculated embedding impedances seen by the diode at the input, idler and output frequencies. Z_d^* and X_d^* are the complex conjugate of the diode impedance and reactance respectively at 250, 450–550 and 750 GHz. M are measured and C are calculated impedances in the figures, except for the idler where "o" = calculated and "x" is measured. The positions of the input and the output backshorts of the tripler are varied over $\lambda_g/2$ in the calculations and in the measurements, where λ_g is the guide wavelength in the respective waveguide. The normalized resistance in the SMITH-charts is 50 Ω. (a) Input frequency, 250 GHz. (b) Idler frequencies, 450, 500, 550 GHz. (c) Output frequency, 750 GHz.

MEASUREMENTS

In the initial test phase a carcinotron was used as the pump source for the 750 GHz tripler. This is however to be replaced with a solid state 250 GHz tripler at a later stage.

The mount was developed for a 2.8 fF varactor diode having a series resistance of 20 Ω. However due to lack of a suitable diode with this capacitance a 5.4 fF varactor diode having a series resistance of 11 Ω and a breakdown voltage V_b of 9 V was tested in the mount. The 5.4 fF diode has nearly the same ωRC constant as the 2.8 fF one and should therefore give close to the same output efficiency, however at a higher input power.

Computer simulations of the tripler using the theoretical model of the mount showed that it is possible to match the 5.4 fF diode, by reducing the whisker length to 50 μm compared to 60 μm for the 2.8 fF device, though with a loss in maximum efficiency. Thus it was found using computer simulations, that a maximum efficiency of 12.8% could be achieved with the 5.4 fF diode in the mount compared to a maximum of 16.3% using optimum embedding impedances, at 750 GHz with 6 mW input power. This can be compared to an efficiency of 18.4% for the 2.8 fF diode at optimum embedding impedances using the same input power. The small difference, that is 16.3–18.4% is mainly due to the difference in cutoff frequency for the devices.

The measured results for the 750 GHz tripler using the 5.4 fF diode are shown in Fig. 4. The output power was measured using a Scientech disc calorimeter model no. 360001. The disc calorimeter has been tested up to frequencies around 900 GHz using carcinotrons as test sources and proven to be quite accurate comparing the reading from the calorimeter with manufacturers data on the carcinotrons. The output power and efficiency are as can be seen in Fig. 4, very sensitive to the input power. The higher input power means that due to the larger rectified ac-current a larger backbias voltage or in this case a smaller forward bias voltage can be used thereby making the diodes work more in the varactor mode, see Fig. 5. Thus the output power and efficiency using this operating point are greater, compare Fig. 4 and 5. The conversion efficiency for the 5.4 fF diode was calculated for 12 mW input power, (peak power in Fig. 4), to be 23%. The calculated mismatch between the diode and the mount at the frequency for maximum output power, i.e., at about 803 GHz, was found to reduce the optimum efficiency to 18%, which can be compared to the measured efficiency of 0.8%. The differences between calculated and measured efficiency is probably most attributed to ohmic losses in conjuction with higher mismatch losses than the theoretically calculated ones. However such effects as current saturation in the diode might also be responsible for a part of the losses [9].

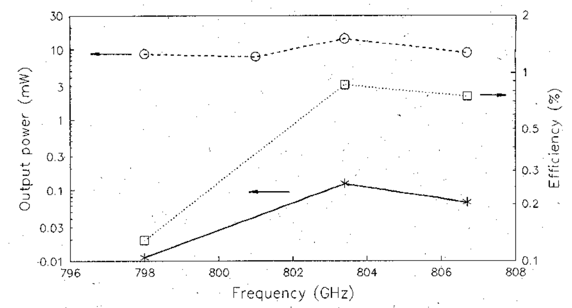

Fig. 4. Measured output power and efficiency for the 750 GHz tripler as a function of the output frequency. The measured output power for the pump source (carcinotron), which is equal to the pump power for the tripler, is also shown. (x): output power from the tripler. (□): efficiency of the tripler. (o): output power from the carcinotron.

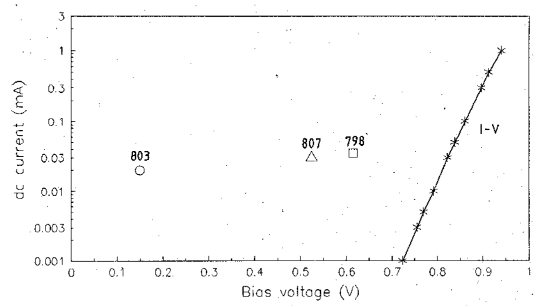

Fig. 5. Measured dc-I–V curve and operating points consisting of the dc-I–V plus the rectified ac-current, for the 5.4 fF diode. The numbers at the operating points refer to the operating frequency in GHz for the particular operating point.

FUTURE WORK

Future work on the 750 GHz tripler will involve testing different Schottky diodes with a $C_j(0)$ between 1.6–3.4 fF in order to find the optimum diode to be used for the frequency range. The investigation of suitable diodes will also involve so-called Single Barrier Varactor SBV-diodes [10]. Due to the symmetrical I–V and C–V characteristic of the SBV-diodes only odd harmonics are generated in these devices [10]. Thus they are particularly suitable for use in triplers since so idler resonator is needed, thereby reducing the losses at the idler frequency to zero [11].

Conclusion

The design and development of a frequency tripler for 750 GHz has been described. State of the art output powers and efficiencies of more than 120 μW and 0.8% respectively has been achieved at 803 GHz using a carcinotron as the test source for the tripler.

Acknowledgments

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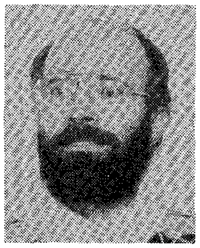

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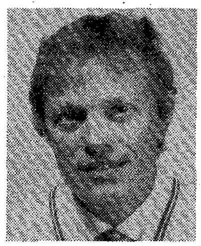

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